Registration No.: .....

BHARTIYA SKILL DEVELOPMENT UNIVERSITY

School of Computing Skills

1st Semester / 2nd In-Sem. Examinations
B. Voc. Program, Summer Semester (2019)

ITN 1101 Introduction to Computers **Time: 1 Hour**

Instruction: Answer all questions **Max. Marks: 20**

Section – A **05X01 = 05 Marks**

1. Which one of the following refers to GUI?
   i) Graphical User Interface
   ii) Graphically Used Interface
   iii) Geographic Unit Interface
   iv) None of the Above
2. Which one of the following refers to ROM?
   i) Read Only Memory
   ii) Read Access Memory
   iii) Read Arithmetic Memory
   iv) Random Arithmetic Memory
3. Which one of the following is the longest key on the keyboard?
   i) Enter Key
   ii) Tab Key
   iii) Space Bar
   iv) Backspace Key
4. Which of the following represents a Desktop PC with monitor stacked on top of system unit?
   i) Horizontal Oriented System ii) Vertical Oriented System iii) Flat Oriented System iv) Circular Oriented System
5. Which of the following refers to software that are used to drive microprocessor based systems?
   i) Assembly Language Programs ii) Firmware iii) Flowchart Instructions iv) Basic Interpreter Instructions

Section – B **03x02=06 Marks**

1. Explain the functioning of Full Adder.

2. Explain the Pin Diagram of 8085 Microprocessor

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3. Calculate using Binary Division:
   i) 10110.1 divided by 1101
   ii) 101.11 divided by 111
   iii) 11101.01 divided by 1100

Section – C **03X03 = 09 Marks**

1. Explain the OSI Model in Detail.

2. Explain the various Secondary Storage Devices with the help of examples.

3. Explain JK and T Flip Flops using State and Characteristic Tables.

School of Computing Skills

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Instruction: Answer all questions **Max. Marks: 20**

Section – A

Ans. 1: (i) Graphical User Interface

Ans. 2: (i) Read Only Memory

Ans. 3:(iii) Space Bar

Ans. 4: (i) Horizontal Oriented System

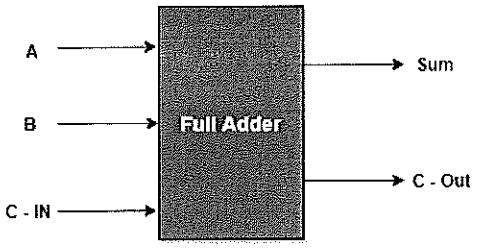
Ans. 5: (i) Assembly Level Programs

Section – B

Ans. 1:

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

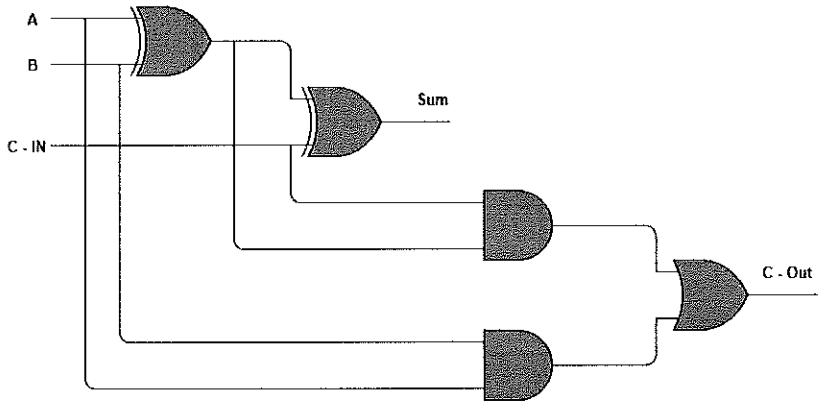
A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.

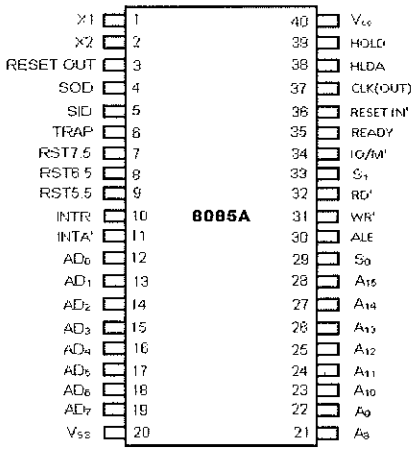


Full Adder Truth Table:

Inputs			Outputs	
A	B	C – IN	Sum	C- Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder Circuit Diagram:





Ans: 2

Ans-2.

1. Address Bus and Data Bus:
The address bus is a group of sixteen lines i.e A0-A15. The address bus is unidirectional, i.e., bits flow in one direction from the microprocessor unit to the peripheral devices and uses the high order address bus.

2. Control and Status Signals:

- **ALE** – It is an Address Latch Enable signal. It goes high during first T state of a machine cycle and enables the lower 8-bits of the address, if its value is 1 otherwise data bus is activated.
- **IO/M'** – It is a status signal which determines whether the address is for input-output or memory. When it is high(1) the address on the address bus is for input-output devices. When it is low(0) the address on the address bus is for the memory.
- **SO, S1** – These are status signals. They distinguish the various types of operations such as halt, reading, instruction fetching or writing.

- **RD'** – It is a signal to control READ operation. When it is low the selected memory or input-output device is read.
- **WR'** – It is a signal to control WRITE operation. When it goes low the data on the data bus is written into the selected memory or I/O location.
- **READY** – It senses whether a peripheral is ready to transfer data or not. If READY is high(1) the peripheral is ready. If it is low(0) the microprocessor waits till it goes high. It is useful for interfacing low speed devices.

3. Power Supply and Clock Frequency:

- **Vcc** – +5v power supply
- **Vss** – Ground Reference
- **XI, X2** – A crystal is connected at these two pins. The frequency is internally divided by two, therefore, to operate a system at 3MHZ the crystal should have frequency of 6MHZ.
- **CLK (OUT)** – This signal can be used as the system clock for other devices.

4. Interrupts and Peripheral Initiated Signals:
The 8085 has five interrupt signals that can be used to interrupt a program execution.

(i) INTR
(ii) RST 7.5
(iii) RST 6.5
(iv) RST 5.5
(v) TRAP

The microprocessor acknowledges Interrupt Request by INTA' signal. In addition to Interrupts, there are three externally initiated signals namely RESET, HOLD and READY. To respond to HOLD request, it has one signal called HLDA.

- **INTR** – It is an interrupt request signal.
- **INTA'** – It is an interrupt acknowledgment sent by the microprocessor after INTR is received.

5. Reset Signals:

- **RESET IN'** – When the signal on this pin is low(0), the program-counter is set to zero, the buses are tristated and the microprocessor unit is reset.
- **RESET OUT** – This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

6. DMA Signals:

- **HOLD** – It indicates that another device is requesting the use of the address and data bus. Having received HOLD request the microprocessor relinquishes the use of the buses as soon as the current machine cycle is completed. Internal processing may continue. After the removal of the HOLD signal the processor regains the bus.
- **HLDA** – It is a signal which indicates that the hold request has been received after the removal of a HOLD request, the HLDA goes low.

7. Serial I/O Ports:
Serial transmission in 8085 is implemented by the two signals,

- **SID and SOD** – SID is a data line for serial input where as SOD is a data line for serial output.

Ans.3. (i) 1.10111011

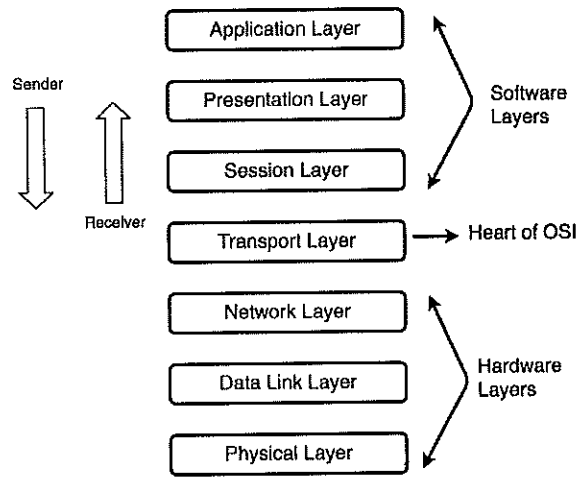
(ii) 0.1101001

(iii) 10.0111

Section – C

Ans.1:

OSI stands for **Open Systems Interconnection**. It has been developed by ISO – **'International Organization of Standardization'**, in the year 1974. It is a 7 layer architecture with each layer having specific functionality to perform. All these 7 layers work collaboratively to transmit the data from one person to another across the globe.



1. Physical Layer (Layer 1) : The lowest layer of the OSI reference model is the physical layer. It is responsible for the actual physical connection between the devices. The physical layer contains information in the form of **bits.** It is responsible for the actual physical connection between the devices. When receiving data, this layer will get the signal received and convert it into 0s and 1s and send them to the Data Link layer, which will put the frame back together.

2. Data Link Layer (DLL) (Layer 2) : The data link layer is responsible for the node to node delivery of the message. The main function of this layer is to make sure data transfer is error free from one node to another, over the physical layer. When a packet arrives in a network, it is the responsibility of DLL to transmit it to the Host using its MAC address.
Data Link Layer is divided into two sub layers :

1. Logical Link Control (LLC)
2. Media Access Control (MAC)

3. Network Layer (Layer 3) : Network layer works for the transmission of data from one host to the other located in different networks. It also takes care of packet routing i.e. selection of the shortest path to transmit the packet, from the number of routes available. The sender & receiver's IP address are placed in the header by network layer.
The functions of the Network layer are :

1. **Routing:** The network layer protocols determine which route is suitable from source to destination. This function of network layer is known as routing.
2. **Logical Addressing:** In order to identify each device on internetwork uniquely, network layer defines an addressing scheme. The sender & receiver's IP address are placed in the header by network layer. Such an address distinguishes each device uniquely and universally.

4. Transport Layer (Layer 4) : Transport layer provides services to application layer and takes services from network layer. The data in the transport layer is referred to as *Segments*. It is responsible for the End to End delivery of the complete message. Transport layer also provides the acknowledgment of the successful data transmission and re-transmits the data if an error is found.

5. Session Layer (Layer 5) :

This layer is responsible for establishment of connection, maintenance of sessions, authentication and also ensures security.
The functions of the session layer are :

1. **Session establishment, maintenance and termination:** The layer allows the two processes to establish, use and terminate a connection.
2. **Synchronization :** This layer allows a process to add checkpoints which are considered as synchronization points into the data. These synchronization point help to identify the error so that the data is re-synchronized properly, and ends of the messages are not cut prematurely and data loss is avoided.
3. **Dialog Controller :** The session layer allows two systems to start communication with each other in half-duplex or full-duplex.

6. Presentation Layer (Layer 6) :

Presentation layer is also called the **Translation layer**.The data from the application layer is extracted here and manipulated as per the required format to transmit over the network.
The functions of the presentation layer are :

1. **Translation :** For example, ASCII to EBCDIC.
2. **Encryption/ Decryption :** Data encryption translates the data into another form or code. The encrypted data is known as the cipher text and the decrypted data is known as plain text. A key value is used for encrypting as well as decrypting data.
3. **Compression:** Reduces the number of bits that need to be transmitted on the network.

7. Application Layer (Layer 7) :

At the very top of the OSI Reference Model stack of layers, we find Application layer which is implemented by the network applications. These applications produce the data, which has to be transferred over the network. This layer also serves as a window for the application services to access the network and for displaying the received information to the user.

Ans 2.

Secondary storage technology refers to storage devices and storage media that are not always directly accessible by a computer. This differs from primary storage technology, such as an internal hard drive, which is constantly available.

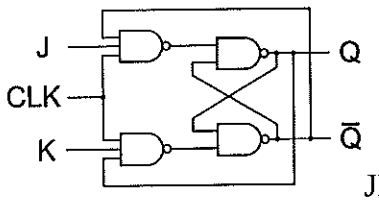
Examples of secondary storage devices include external hard drives, USB flash drives, and tape drives. These devices must be connected to a computer's external I/O ports in order to be accessed by the system. They may or may not require their own power supply.

Examples of secondary storage media include recordable CDs and DVDs, floppy disks, and removable disks, such as Zip disks and Jaz disks. Each one of these types of media must be inserted into the appropriate drive in order to be read by the computer. While floppy disks and removable disks are rarely used anymore, CDs and DVDs are still a popular way to save and transfer data.

Because secondary storage technology is not always accessible by a computer, it is commonly used for archival and backup purposes. If a computer stops functioning, a secondary storage device may be used to restore a recent backup to a new system. Therefore, if you use a secondary storage device to backup your data, make sure you run frequent backups and test the data on a regular basis.

Ans. 3.

JK Flip Flop Due to the undefined state in the SR flip flop, another flip flop is required in electronics. The JK flip flop is an improvement on the SR flip flop where S=R=1 is not a problem.



JK Flip-Flop

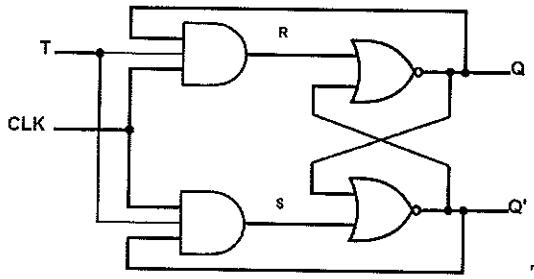
The input condition of J=K=1, gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically.

In simple words, If J and K data input are different (i.e. high and low) then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge then the output will toggle from one state to the other. JK Flip Flop can function as Set or Reset Flip flop

J	**K**	**Q**	**Q'**
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	1
0	1	1	0
1	0	1	1
1	1	1	0

T Flip Flop

A T flip flop is like JK flip-flop. These are basically a single input version of JK flip flop. This modified form of JK flip-flop is obtained by connecting both inputs J and K together. This flip-flop has only one input along with the clock input.



T Flip-Flop

These flip-flops are called T flip-flops because of their ability to complement its state (i.e.) Toggle, hence the name Toggle flip-flop.

T	**Q**	**Q (t+1)**
0	0	0
1	0	1
0	1	1
1	1	0

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Registration No.: .....

School of Computing Skills
Session: 2019-20 (Summer)
B. Voc. Program, 1st Semester,
IInd In-Sem. Examination

ITN1104
Basic Computer Networking
Instruction: Answer all Questions

Time: 1 Hour
Max. Marks: 20

Section – A Marks 05X01 = 05

Q1. Which one of the following CRC stands for?
a) cyclic redundancy check
b) code repeat check
c) code redundancy check
d) cyclic repeat check

Q2. Which one of the following a Header of a frame generally contains?
a) synchronization bytes
b) addresses
c) frame identifier
d) all of the mentioned

Q3. Which one of the following is the type of error when 2 or more bits in a data unit has been changed during the transmission?
a) random error
b) burst error
c) inverted error
d) none of the mentioned

Q4. Which one of the following layer provides packets to data link layer which encapsulates them into frames for transmission?
a) network layer
b) physical layer
c) transport layer
d) application layer

Q5. Which one of the following task is not done by data link layer?
a) framing
b) error control
c) flow control
d) channel coding

Section – B Marks 03X02 = 06

Q1. The message 11001001 is to be transmitted using the CRC polynomial x^3 + 1 to protect it from errors. Write the message that should be transmitted. Show all the steps involved.

Q2 What advantages does fiber optics have over other media?

Q3. Mention the function of go-back N-ARQ.

Section – C Marks 03X03 = 09

Q1. Define ARQ.
Q2. What are the responsibilities of data link layer?
Q3. What is a buffer?

Answer Key

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Semester- 1, IInd In-Sem Examination

B. Voc. Program, Summer (2019-20)

ITN 1104 **Time: 1 Hour**

Basic Computer Networking **Max. Marks: 20**

Instruction: Answer All Questions

Section - A

A1. a
A2. d
A3. b
A4. a
A5. d

Section – B

A1. 11001001011

The polynomial x^3+1 corresponds to divisor is 1001.

```
11001001 000  <--- input right padded by 3 bits
1001          <--- divisor
01011001 000  <---- XOR of the above 2
 1001         <--- divisor
00010001 000
  1001
00000011 000
    10 01
00000001 010
     1 001
00000000 011 <------ remainder (3 bits)
```

Put the remainder in the end of the data and send.

A2. One major advantage of fiber optics is that is it less susceptible to electrical interference. It also supports higher bandwidth, meaning more data can be transmitted and received. Signal degrading is also very minimal over long distances.

A3. It is the popular mechanism for continuous transmission error control. In the method, if our frame is lost or damaged, all frames sent since the last frame acknowledged are retransmitted.

Section – C

A1. Error control in the data link layer is based on Automatic repeat request (ARQ),

which means retransmission of data in 3 cases.

1. Damaged frame
2. Lost frame
3. Lost acknowledgment.

A2. Specific responsibilities of data link layer include the following.

a) Framing
b) Physical addressing
c) Flow control
d) Error control
e) Access control

A3. Each receiving device has a block of memory called a buffer, reserved for storing incoming data until they are processed.

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Bhartiya Skill Development University
School of & Networking
1st Semester / 2nd In-Sem. Examinations
B. Voc. Program, Summer/Winter Semester (2018-19)

ITN1105 Operating Systems

Time: 1 Hour

Max. Marks: 20

Instructions: Attempt all questions.

Section-A **(5x1) =05 Marks**

1. Which one of the following in UNIX identifies each process?

a) Process Control Block
b) Device Queue
c) Process Identifier
d) none of the mentioned

2. Which one of the following is used to create a file?

a) allocate the space in file system
b) make an entry for new file in directory
c) allocate the space in file system & make an entry for new file in directory
d) none of the mentioned

3. Which one of the following is indication for caching?

a) Holds a copy of the data
b) Is fast memory
c) Holds the only copy of the data
d) Holds aoutput for a device

4. Which one of the following indicates system performance of I/O?

a) Major Factor
b) Minor Factor
c) Does not matter
d) None of the above

5. Which one of the following defines time quantum?
a) Shortest job scheduling algorithm
b) Round Robin scheduling algorithm
c) Priority scheduling algorithm
d) Multilevel queue scheduling algorithm

Section-B **(3x2) = 06 Marks**

Q1. What is difference between shell and kernel?

Q2. What is root account?

Q3. Write 4 commands used in command line prompt?

Section-C **(3x3) = 09 Marks**

Q1. What are the approaches to communicate between CPU and device?

Q2. What is polling I/O and Interrupts I/O?

Q3. What is system threats and describe its types?

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B. Voc. Program, Summer/Winter Semester (2018-19)

ITN1105 Operating Systems **Time: 1 Hour**

Max. Marks: 20

Instructions: Attempt all questions.

Section-A **(5x1) =05 Marks**

1. Which one of the following in UNIX identifies each process?

a) Process Control Block
b) Device Queue
c) Process Identifier
d) none of the mentioned Ans a)

2. Which one of the following is used to create a file?

a) allocate the space in file system
b) make an entry for new file in directory
c) allocate the space in file system & make an entry for new file in directory
d) none of the mentioned ans. a)

3. Which one of the following is full form of ntp?

a) Network Time Protocol
b) No Time Protocol
c) Network Total Protocol
d) None of the above ans. a)

4. Which one of the following indicates the effect on system performance of I/O?

a) Major Factor
b) Minor Factor
c) Does not matter
d) None of the above ans. a)

5. Which one of the following is not true?
a) kernel is the program that constitutes the central core of the operating system
b) kernel is the first part of operating system to load into memory during booting
c) kernel is made of various modules which cannot be loaded in running operating system
d) kernel remains in the memory during the entire computer session **Ans. c)**

Section-B **(3x2) = 06 Marks**

Q1. What is difference between shell and kernel?

Ans. The main difference between kernel and shell is that the kernel is the core of the operating system that controls all the tasks of the system while the shell is the interface that allows the users to communicate with the kernel.

Q2. What is root account?

Ans. The root is the user name or account that by default has access to all commands and files on a Linux or other Unix-like operating system. It is also referred to as the root account, root user, and the superuser.

Q3. Write commands for creating file, writing text in file, opening a file and deleting a file.

Ans. Creating file: cat< myfirst file, writing text in file: vi <filename>, opening a file:cat <filename>, deleting a file : rm <filename>

Section-C **(3x3) = 09 Marks**

Q1.How CPU and I/O devices communicate? Explain in detail.

Ans. The communication between CPU and input/output devices is implemented using an interface unit. In a computer system, data is transferred from an input device to the processor and from the processor to an output device. Each input and output device is provided with a device controller, which is used to manage the working of various peripheral devices. Actually, the CPU communicates with the device controllers for performing the I/O operations.

Q2. What are different functions of operating system?

Ans. An Operating System (OS) is an interface between a computer user and computer hardware. An operating system is a software which performs all the basic tasks like file management, memory management, process management, handling input and output, and controlling peripheral devices such as disk drives and printers.

Q3. What is system thread and describe its types?

Ans. Thread is a single sequence stream within a process. Threads have same properties as of the process so they are called as light weight processes. Threads are executed one after another but gives the illusion as if they are executing in parallel. Each thread has different states. Each thread has

1. A program counter
2. A register set
3. A stack space

Threads are not independent of each other as they share the code, data, OS resources etc.